REMARKS

Claims 7-18 are currently pending in the application. Claims 7 and 15 are independent claims and claims 8-14 and 16-18, respectively, depend from the independent claims. Claims 7 and 13-15 have been amended to correct minor typographical errors without narrowing the scope of the claims. The Applicants request reconsideration of the pending claims in light of the amendments above and the remarks recited below.

Claim 7 was objected to because of a minor informality. Applicants respectfully traverse the objection but have amended claim 7 to overcome the objection without narrowing the scope of the claim. Applicants respectfully assert that claim 7 complies with the U.S. patent rules and regulations and therefore is allowable. Applicants assert that objection to claim 7 is now moot and request that objection to claim 7 be withdrawn.

Claims 7-9, 11, 13-16 and 18 were rejected under 35 U.S.C. § 102(e) as being anticipated by Butter et al., U.S. Patent 6,549,575, "Butter". Additionally, claims 10, 12 and 17 were rejected under 35 U.S.C. § 103(a) as being obvious in view of Butter. The Applicants respectfully traverse the rejections. The Applicants respectfully assert that independent claim 7 and 15 are allowable over the cited reference for at least the reasons set forth below.

The Applicants set forth in claim 7 a motion estimation processor. The motion estimation processor comprises a controller and a plurality of resolution processors connected to the controller. The plurality of resolution processors analyze development of a video signal in time and produce motion analysis. The controller also controls the plurality of resolution processors.

According to the Office Action, Butter discloses every feature recited in the Applicants' claim 7. The Applicants respectfully disagree and submit that Butter is different from the Applicants' invention as recited in claim 7.

According to the Office Action, Butter discloses a motion estimation processing unit (331, Figure 8), a full resolution unit (321, Figure 8), a half resolution unit (323, Figure 8), and a memory controller (301, Figure 8), and further according to the Office Action, the recited elements in Butter anticipate the Applicants' claim 7. The Applicants respectfully disagree.

Applicants recite in claim 7 a motion estimation processor comprising a controller. The controller controls the plurality of resolution processors. Butter does not teach or suggest the motion estimation processing unit (331, Figure 8) having a controller. Butter is different from the Applicants' claimed invention as recited in claim 7 at least because Butter does not disclose a motion estimation processor having a controller.

Additionally, because Butter does not teach a motion estimation processor having a controller, Butter is incapable of teaching a motion estimation processor controller controlling a plurality of resolution processors. Instead, Butter merely discloses a memory controller 301. The Applicants respectfully submit that the memory controller as disclosed by Butter is different from the motion estimation processor controller as recited in Applicants' claim 7.

Further, the Applicants recite in claim 7, a plurality of resolution processors analyzing development of a video signal in time and producing motion analysis. The Applicants respectfully submit that Butter does not disclose a plurality of resolution processors as recited in Applicants' claim 7. Further, the Applicants respectfully submit that Butter does not disclose resolution processors analyzing development of a video signal in time and producing motion analysis.

In contrast to the Applicants' claimed invention as recited in claim 7, Butter merely discloses a first motion estimation refinement step being performed in a full resolution (FR) unit 321. The FR unit 321 fetches current macro-block luminance data and reference macro-block luminance data pertaining to a full pixel refinement search window from a refinement search memory via the memory controller unit 301 (col. 8, lines 61-67).

The Applicants' respectfully submit that the FR unit as disclosed by Butter is different from a resolution processor as recited in Applicants' claim 7. Further, the Applicants respectfully assert that the function performed by the FR unit as disclosed in Butter cannot be characterized as analyzing development of a video signal in time and producing motion analysis. Instead, as disclosed by Butter, the FR unit merely performs a single first motion estimation refinement step.

Additionally, Butter discloses a second motion estimation refinement step being performed in a half resolution (HR) unit 323. The HR unit 323 performs a refinement search for up to 8 half pixel reference macro-blocks which surround a best match full pixel reference macro-block as determined by the FR unit 321 (col. 10, lines 11-16).

The Applicants' respectfully submit that the HR unit as disclosed by Butter is different from a resolution processor as recited in Applicants' claim 7. Further, the Applicants respectfully assert that the function performed by the HR unit as disclosed in Butter cannot be characterized as analyzing development of a video signal in time and producing motion analysis. Instead, as disclosed by Butter, the HR unit merely performs a single second motion estimation refinement step.

Furthermore, Butter discloses another motion estimation refinement step being performed in the dual prime (DP) unit 325. The DP unit 325 can be configured to perform dual prime refinement using current macro-block data and reference macro-block data from either the FR unit 321 or the HR unit 323. The Applicants' respectfully submit that the DP unit as disclosed by Butter is different from a resolution processor as recited in Applicants' claim 7. Further, the Applicants respectfully assert that the function performed by the DP unit as disclosed in Butter cannot be characterized as analyzing development of a video signal in time and producing motion analysis. Instead, as disclosed by Butter, the DP unit merely performs a single third motion estimation refinement step.

For at least the reasons set forth above, the Applicants respectfully assert that Butter does not teach , suggest or disclose the features recited in Applicants' claim 7. Therefore, claim 7 is allowable over the cited reference. The Applicants request that rejection of claim 7 over Butter be withdrawn.

Claims 8-14 depend from independent claim 7. Because independent claim 7 is allowable over Butter, the Applicants respectfully submit that dependent claims 8-14 are also allowable over the cited reference. The Applicants assert that the rejection of claims 8-14 is now moot and request that the rejection of dependent claims 8-14 be withdrawn.

The Applicants set forth in claim 15 a digital signal processor for processing a multiple frame video digital signal. The digital signal processor comprises a digital signal processor (DSP) controller, a plurality of processing units are connected to the DSP controller for processing the multiple frame video digital signal, and at least one storage unit. Each of the processing units is connected to at least one storage units. The DSP controller controls the plurality of processing units. The DSP controller, the plurality of processing units, and the at least one storage unit are all on a single chip.

According to the Office Action, Butter discloses every feature recited in the Applicants' claim 15. The Applicants respectfully disagree and submit that Butter is different from the Applicants' invention as recited in claim 15.

Applicants' recite in claim 15, a digital signal processor for processing a multiple frame video digital signal comprising a digital signal processor controller. The digital signal processor controller controls a plurality of processing units. Butter does not teach or suggest a digital signal processor having a digital signal processor controller. Butter is at least different from the Applicants' claimed invention as recited in claim 15 because Butter does not disclose a digital signal processor having a digital signal processor controller.

Additionally, because Butter does not teach a digital signal processor having a digital signal processor controller, Butter is incapable of teaching a digital signal processor controller controlling a plurality of processing units. Instead, Butter merely discloses a memory controller 301. The Applicants respectfully submit that the memory controller as disclosed by Butter is different from the digital signal processor controller as recited in the Applicants' claim 15.

Further, because Butter does not teach a digital signal processor having a digital signal processor controller, Butter is incapable of teaching a plurality of processing units connected to the digital signal processor controller for processing the multiple frame video digital signal. Instead, Butter merely discloses a memory controller 301. The Applicants respectfully submit that the memory controller as disclosed by Butter is different from the digital signal processor controller as recited in the Applicants' claim 15.

Butter is also different from the invention recited in Applicants' claim 7 because Butter does not disclose at least one storage unit. The Office Action has suggested that the at least one storage unit is inherently disclosed. The Applicants respectfully disagree. Because Butter does not perform the same function as the Applicants' invention as recited in claim 15, Butter does not disclose nor have need of at least one storage unit as recited in Applicants' claim 15.

Further, the Applicants set forth in claim 15 that each of the plurality of processing units are connected to the at least one storage unit. Because Butter does not disclose at least one storage unit as set forth in Applicants' claim 15, Butter is incapable of teaching and disclosing a plurality of processing units connected to at least one storage unit.

Butter is also different from the Applicants' invention as recited in claim 15 because Butter does not disclose a digital signal processor controller, a plurality of processing units, and at least one storage unit being on a single chip. The Applicants respectfully assert that Butter discloses a plurality of data bus (for example, SEARCH DATA BUS IN Figure 6 and 7, DIFF/QXFRM DATA BUS in Figures 6 and 8, REFINEMENT DATA BUS in Figures 6 and 8, CMB DATA BUS (LUMA + CHROMA) in Figure 6-8, etc.). The Applicants respectfully assert that Butter teaches away from consolidating all processing components on a single chip in contrast to Applicants' claim 15, wherein the Applicants recite a digital signal processor controller, a plurality of processing units, and at least one storage unit being on a single chip.

For at least the reasons set forth above, the Applicants respectfully assert that Butter does not teach , suggest or disclose the features recited in Applicants' claim 15. Therefore, claim 15 is allowable over the cited reference. The Applicants assert that rejection of claim 15 is now moot and request that rejection of claim 15 over Butter be withdrawn.

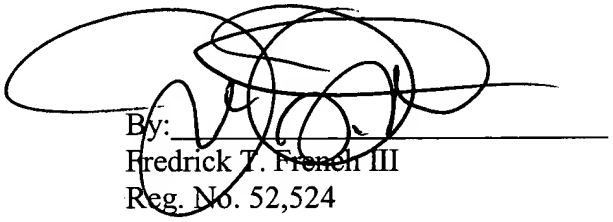
Claims 16-18 depend from independent claim 15. Because independent claim 15 is allowable over Butter, the Applicants respectfully submit that dependent claims 16-18 are also allowable over the cited reference. The Applicants request that rejection of dependent claims 16-18 be withdrawn.

CONCLUSION

Based on at least the foregoing, the Applicants believe that claims 7-18 are in condition for allowance. If the Examiner disagrees or has any question regarding this submission, the Applicants request that the Examiner telephone the undersigned at (312) 775-8000.

A Notice of Allowance is courteously solicited.

Respectfully submitted,



Dated: March 2, 2004

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